Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **NULL**
2. **–INPUT**
3. **+INPUT**
4. **V-**
5. **NC**
6. **OUTPUT**
7. **V+**
8. **NULL**

**1**

**2**

**3**

**4**

**8**

**7**

**6**

**MASK**

**REF**

**1427S**

**.065”**

**.094”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 1427S**

**APPROVED BY: DK DIE SIZE .065” X .094” DATE: 11/15/22**

**MFG: ANALOG DEVICES THICKNESS .021” P/N: OP27NBC**

**DG 10.1.2**

#### Rev B, 7/19/02